AMENDMENTS TO THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) A method for synchronizing a data signal and a clock signal, comprising:

   generating a first intermediate data signal that lags the data signal;

   generating a second intermediate data signal that lags the first intermediate data signal; and

   generating an output signal that combines the duration of the first intermediate data signal and the duration of the second intermediate data signal, wherein the output signal is synchronized with the clock signal, wherein generating the output signal is controlled by a synchronization signal.

2. (Cancelled)

3. (Currently Amended) The method of claim [[2]] 1, wherein the synchronization signal controls the output signal with a multiplexor.

4. (Original) The method of claim 1, wherein the first intermediate data signal is generated by a flip-flop.

5. (Cancelled)

6. (Original) The method of claim 1, wherein the second intermediate data signal is generated by a latch.

7. (Original) The method of claim 1, wherein the second intermediate data signal lags the first intermediate data signal by one half of a clock cycle.

8. (Currently Amended) The method of claim [[2]] 1, wherein the synchronization signal is activated after the second intermediate data signal is generated.

9. (Currently Amended) A method for synchronizing a data signal and a clock signal, comprising:

step of generating a first intermediate data signal that lags the data signal;

step of generating a second intermediate data signal that lags the first intermediate data signal; and

step of synchronizing the data signal with the clock signal by combining the duration of the first intermediate data signal and the duration of the second intermediate data signal, wherein the step of synchronizing is controlled by a synchronization signal.

10. (Currently Amended) An apparatus for synchronizing a data signal and a clock signal, comprising:

a first data storage device that generates a first intermediate data signal that lags the data signal;

a second data storage device that generates a second intermediate data signal that lags the first intermediate data signal; and

a multiplexor that generates an output signal that combines the duration of the first intermediate data signal and the duration of the second intermediate data signal, wherein the output signal is synchronized with the clock signal, wherein the multiplexor is controlled by a synchronization signal.

11. (Original) The apparatus of claim 10, wherein the first data storage device is a flip-flop.

12. (Cancelled)

13. (Original) The apparatus of claim 10, wherein the second intermediate data signal lags the first intermediate data signal by one half of a clock cycle.

14. (Cancelled)

15. (Currently Amended) The apparatus of claim [[14]] 10, further comprising:

a synchronization control signal generator that delays generation of the synchronization signal until after generation of the second intermediate data signal.

16. (Original) The apparatus of claim 10, further comprising:

a scanning input device that scans a test pattern to the second data storage device during a testing operation.

17. (Original) The apparatus of claim 16, wherein the scanning input device is a multiplexor.

18. (Original) The apparatus of claim 17, wherein the multiplexor is controlled by a scanning enablement signal.

19. (Currently Amended) An apparatus for synchronizing a data signal and a clock signal, comprising:

means for generating a first intermediate data signal that lags the data signal;

means for generating a second intermediate data signal that lags the first intermediate data signal;

and means for generating an output signal that combines the duration of the first intermediate data signal and the duration of the second intermediate data signal, wherein the output signal is synchronized with the clock signal, wherein the means for generating the output signal is controlled by a synchronization signal.

20. (Original) The apparatus of claim 19, further comprising: means for scanning in a test data sequence.